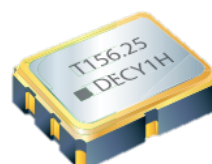


Product Features

- Output Frequency: 15~2100 MHz
- Frequency Stability :
 $\pm 30 \text{ ppm @ } (-40 \sim 85^{\circ}\text{C})$
 $\pm 50 \text{ ppm @ } (-40 \sim 105^{\circ}\text{C})$
- Supply Voltage : 2.5 , 3.3V (Typ.)
- Output Type : LVPECL
- Phase Jitter:
 $0.15\text{fs (Typ.) @156.25MHz LVPECL, } 25^{\circ}\text{C}$
- High Power Supply Noise Rejection Performance
- Industry Standard Package:
 $7.0 \times 5.0 \times 1.7 \text{ mm}$

Application :

- Optical Modules
- High Speed Network Interface Cards
- Data Center Switch



● Table 1 . Electrical Specifications

Test condition
 Ambient temperature: $25 \pm 5^{\circ}\text{C}$
 Relative humidity: 40% ~ 70%

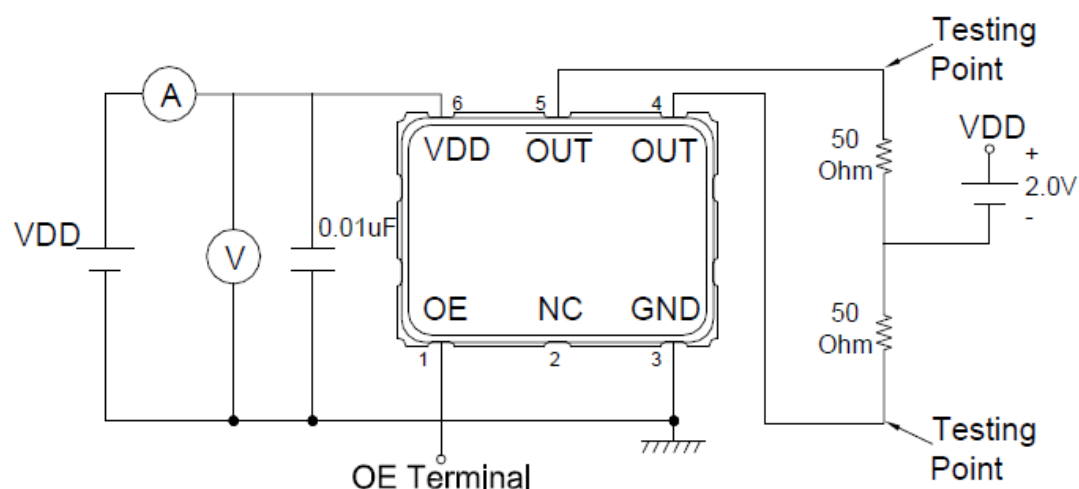
Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions & Notes
Nominal Frequency	F	15~2100			MHz	LVPECL
Frequency Stability	ST	± 30			ppm	@ -40~85°C, Note 1
		± 50				@ -40~105°C, Note 1
Operating Temperature	Topr	-40	-	85	°C	
		-40	-	105		
Supply Voltage	Vdd	2.5 , 3.3 (± 10%)			V	
Symmetry	TH/T	45	50	55	%	
Start-up Time	Tosc	-	-	10	ms	To 90% of Final Amplitude
Current Consumption	Icc	-	93	106	mA	RL=50Ωto VDD-2V
Standby Current	Icc(ST)	-	91	104	uA	OE = Low
Output Voltage High	VoH	Vdd-1.165	-	Vdd-0.8	V	
Output Voltage Low	VoL	Vdd-2.0	-	Vdd-1.555	V	
Output Voltage Range	Vdiff	600	1400	2000	mV	Differential Peak-to-Peak
Rise/ Fall Time	Tr/ Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7xVdd	-	-	V	Note 2 , (Logic1)
Enable Voltage Low	-	-	-	0.3xVdd	V	Note 2, (Logic0)
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.15~0.2	0.25	ps	Integrated from 12KHz~ 20MHz @156.25MHz , 3.3V , Note 3

Note 1 : Inclusive of frequency tolerance at 25°C , variation over temperature , supply voltage variation , 10 years aging and vibration.

Note 2 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.

Note 3 : Phase Jitter will be slightly different according to output frequency and supply voltage.

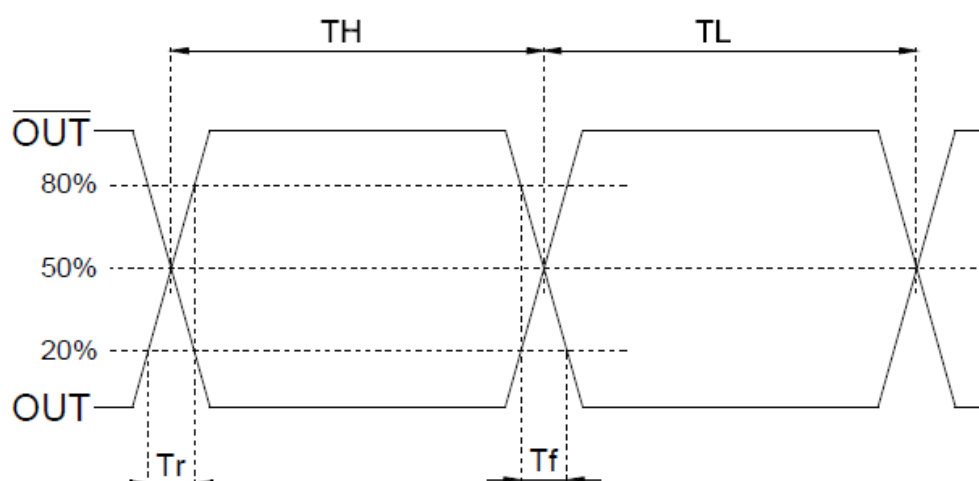
● Test Diagram



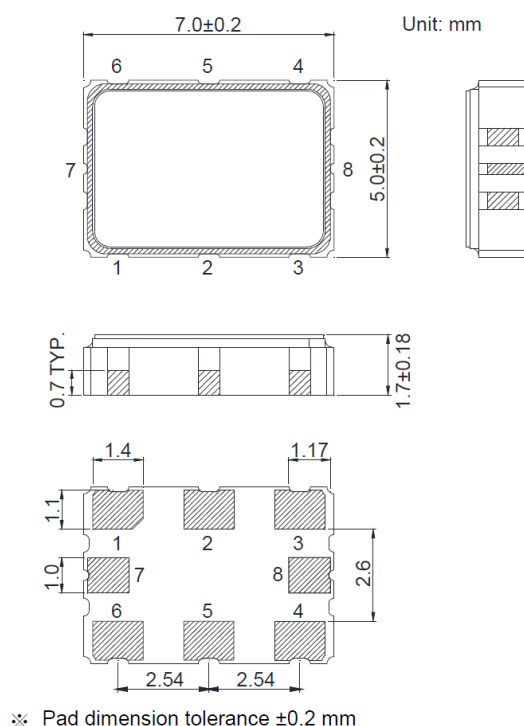
Testing Circuit Note:

1. Above testing circuits cover all the specifications except temperature test & Jitter measurement.
2. All of the testing equipment are 50 Ohm terminal.
3. OE terminal is open connection except OE function test..

● Waveform Conditions



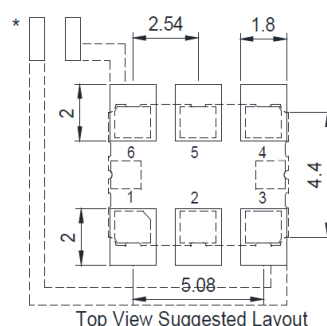
● Dimensions & Footprint (Recommended)



Pin Function:

- | | |
|----------------------------|-------|
| 1. OE | 7. NC |
| 2. NC | 8. NC |
| 3. GND | |
| 4. OUT | |
| 5. $\overline{\text{OUT}}$ | |
| 6. VDD | |

Land Pattern:



※ Power Supply Decoupling Capacitor is Required.

※ Pad dimension tolerance ± 0.2 mm